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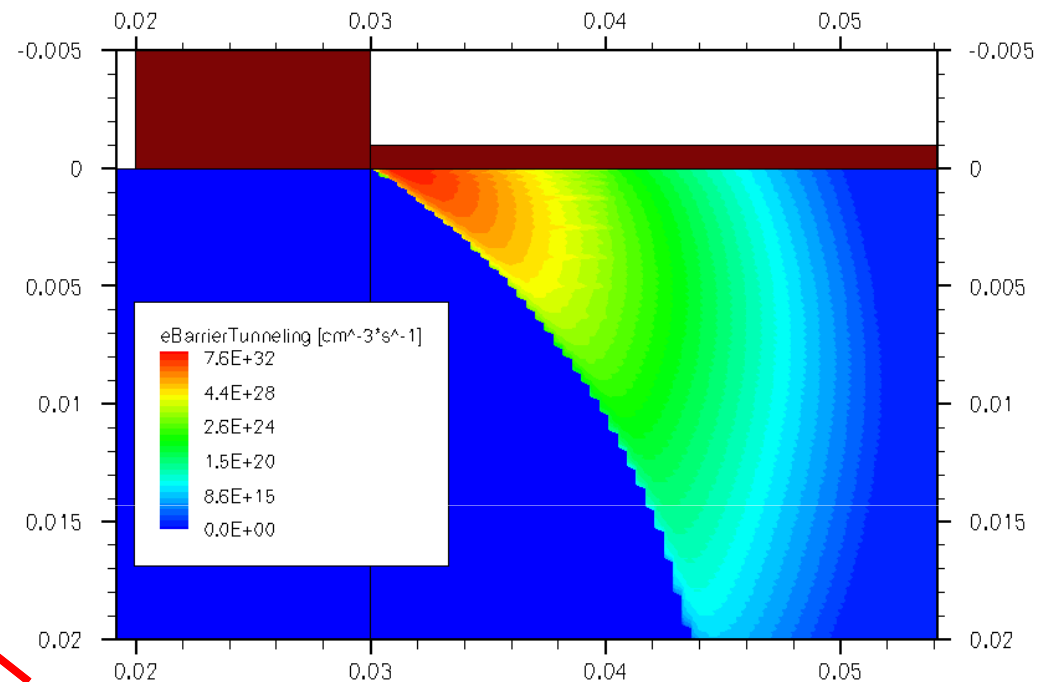
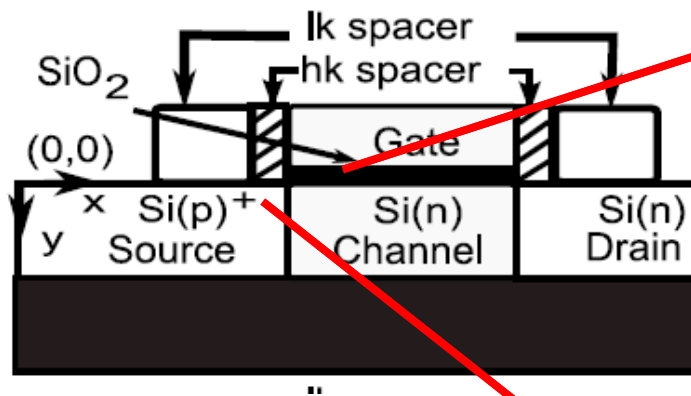
# Impact of electron velocity on the $I_{ON}$ of n-TFETs

David Esseni – University of Udine-IUNET

Many thanks to: H.Virani<sup>1</sup>, P.Palestri<sup>2</sup>, L.Selmi<sup>2</sup>, A. Kottantharayil<sup>1</sup>

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# Context and motivation of this study



- $I_{on}$  boosters focussed on tunneling generation rate at the source (III-V materials, bandgap engineering, high-k spacers, strain, ....)
  - Electrons generated at the source must be drained out and affect the band edges profile along the channel
  - **Can the carrier transport in the channel affect  $I_{on}$ ?**

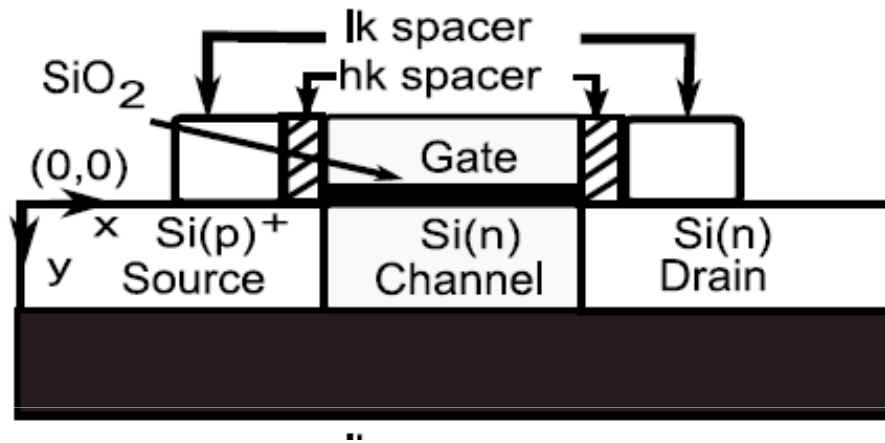


# Outline

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- **Device structure, TCAD models and calibration**
- Impact of electron velocity: a toy model example
- Impact of electron velocity: engineered Si TFETs
- Conclusions

# Device structure and TCAD models



## ■ Single-gate SOI *n*-TFET

- $L_G=50\text{nm}$ ,  $t_{\text{fox}}=1.1\text{nm}$  ( $\text{SiO}_2$ )
- $N_A=10^{17}\text{cm}^{-3}$
- $T_{\text{SI}}=20\text{nm}$ ,  $T_{\text{box}}=10\text{nm}$  ( $\text{SiO}_2$ )
- $N_{\text{SRC}}=10^{20}\text{cm}^{-3}$  peak value
- $N_{\text{DR}}=10^{18}\text{cm}^{-3}$  peak value
- Decay of SD doping 1dec/2nm

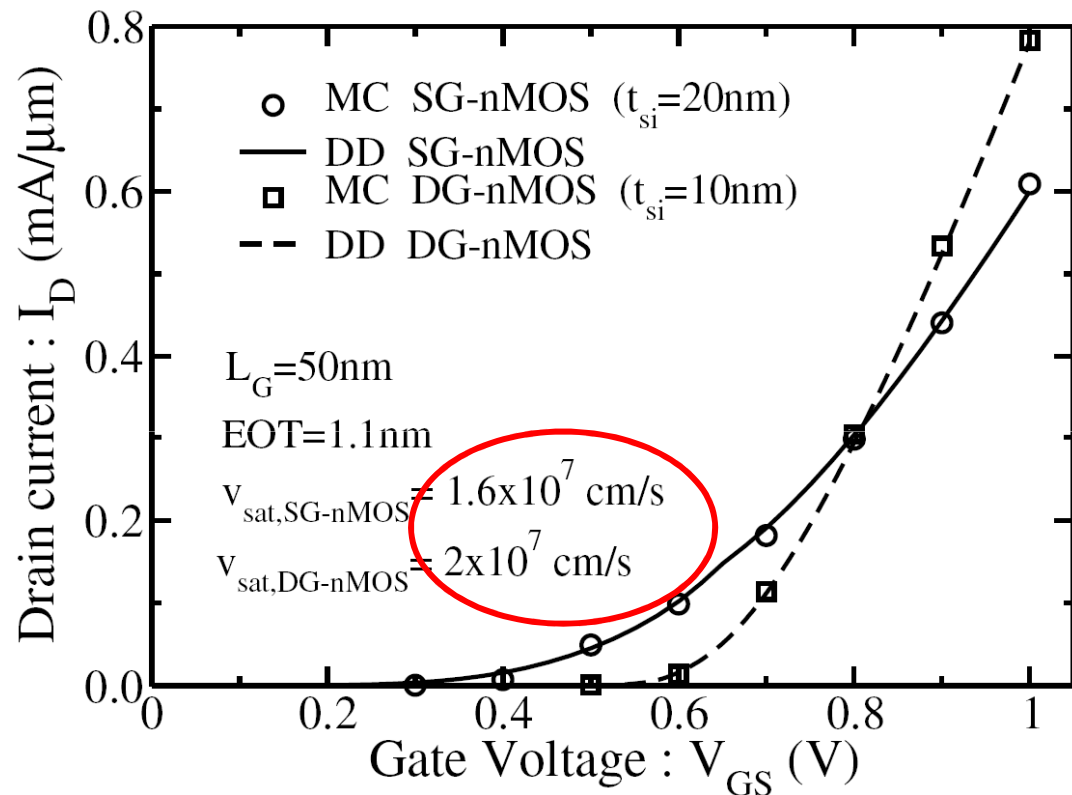
## ■ DESSIS-SENTAURUS simulations

- Drift-diffusion model (calibration)
- Non local BTBT model (calibration)

# Calibration of the Drift Diffusion model

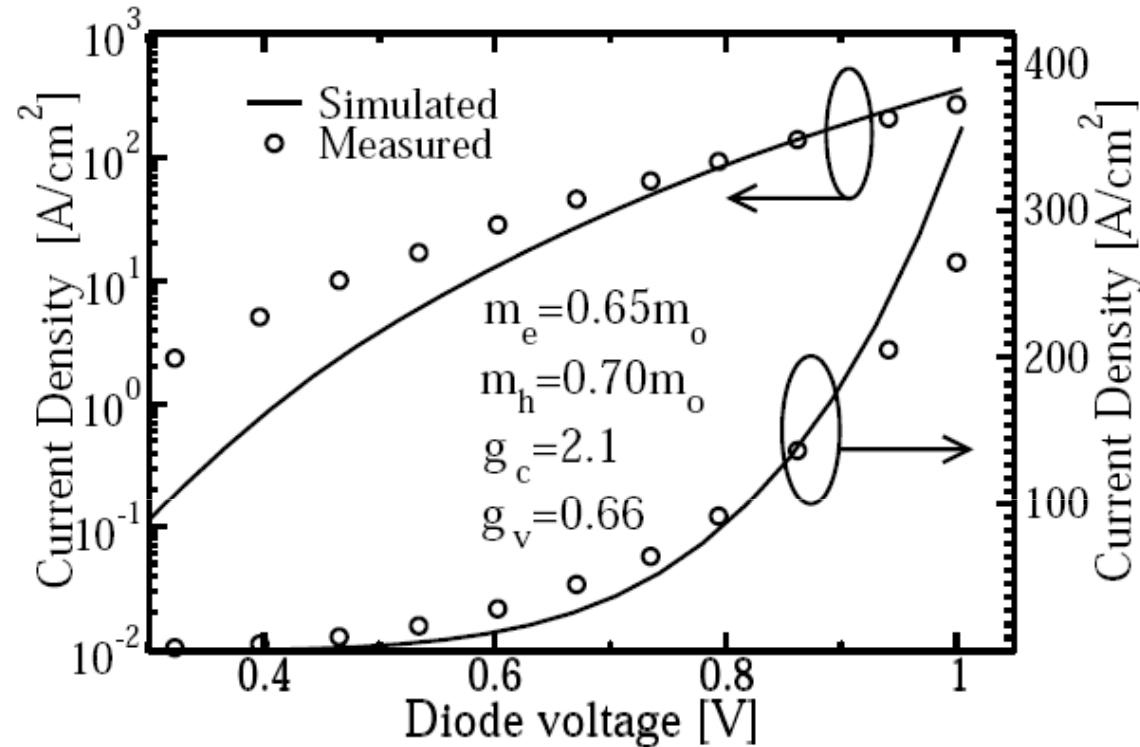
$$v(F) = \frac{\mu_0}{\left[1 + \left(\frac{F\mu_0}{v_{sat}}\right)^\beta\right]^{\frac{1}{\beta}}}$$

- Drift diffusion model calibrated to multi-subband Monte Carlo simulations MOSFET with  $L_G=50\text{nm}$



- Velocity saturation ( $v_{sat}$ ) adjusted in *Caughey-Thomas* velocity versus field relation (J.Bude, SISPAD 2000)

# Calibration of the Tunneling model



- Non local Tunneling model has been calibrated to experimental data for reverse-biased diodes [P. M. Solomon et al. JAP, vol. 95, No. 10, May 2004] ( $g_c$  and  $g_v$  at the default value)

# Resulting simulated $I_{ON}$ values

- Resulting simulated  $I_{ON}$  of about  $0.1\mu\text{A}/\mu\text{m}$  for  $V_{GS} = V_{DS} = 1\text{V}$

Ref	structure	mode of operation	Channel length (nm)	Gate material	EOT (nm)	$V_{DS}$ (V)	$V_{GS}$ (V)	$I_{on}$ ( $\mu\text{A}/\mu\text{m}$ )	$I_{off}$ (pA/ $\mu\text{m}$ )	SS (mV/dec)
[17]	vertical pTFET	p-channel	70	$\text{p}^+$ poly	4.5( $\text{SiO}_2$ )	0.7	-4.5	1	1	>100
[5]	lateral nTFET	n-channel	70	-	2( $\text{SiO}_2$ )	1	1	12	5000	52.8
[7]	gated $\text{p}^+$ -n diode	n-channel	50	$\text{n}^+$ poly	4( $\text{SiO}_2$ )	-3	3	0.001	1	$\approx 50$
[18]	Fin-TFET	p-channel	65	TiN	1.6(EOT)	-2	-2	0.004	-	>100
[9]	lateral strained	n-channel	1000	poly	-	-	5	0.01	800	>100
[8],[19]	lateral	p-channel	100	TiN	3( $\text{HfO}_2$ )	-1	-2.5	0.05	1	42

17- K. K. Bhuvalka *et al.*, *Jap. J. Appl. Phys.*, pp. 3106–3109, 2006.

5- W. Y. Choi *et al.*, *IEEE Elec. Dev. Lett.*, pp. 742–745, 2007.

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18- M. Fulde *et al.*, *2nd IEEE International Nanoelectronics Conference (INEC 2008)*, March 2008, pp. 579–584.

8- F. Mayer *et al.*, in *Tech. Dig. IEDM*, 2008, pp. 163–166.

9- T. Krishnamohan *et al.*, *Tech. Dig. IEDM*, pp. 947–949.

19- C.L.Royer and F.Mayer, *10th International Conference on Ultimate Integration of Silicon*, 2009, March 2009, pp. 53–56.



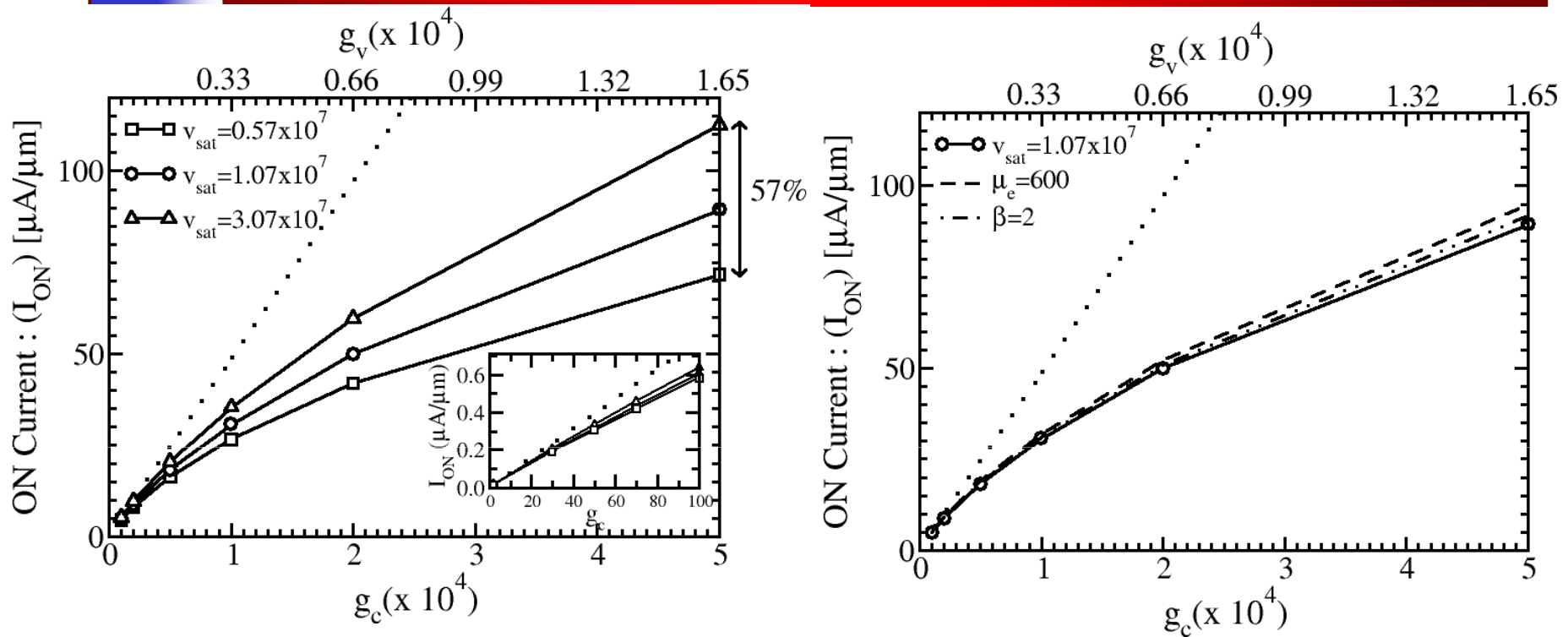
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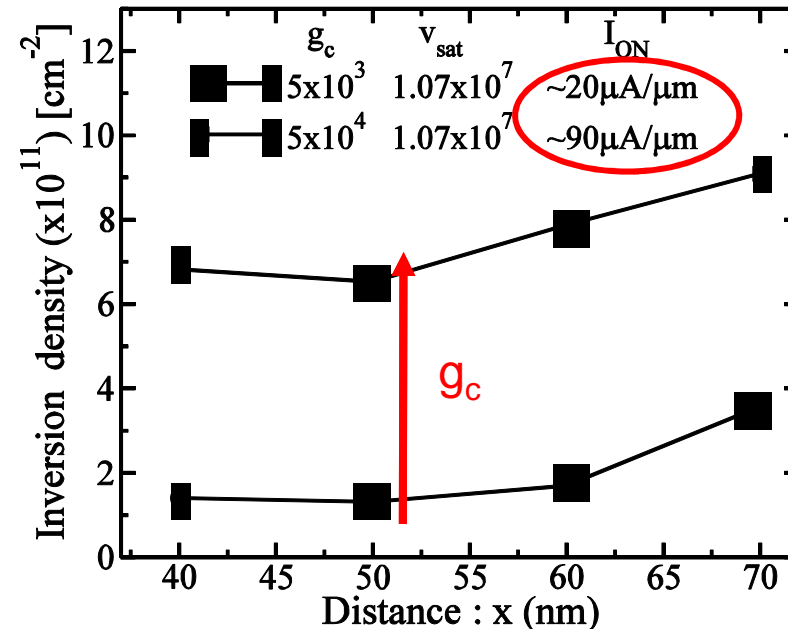
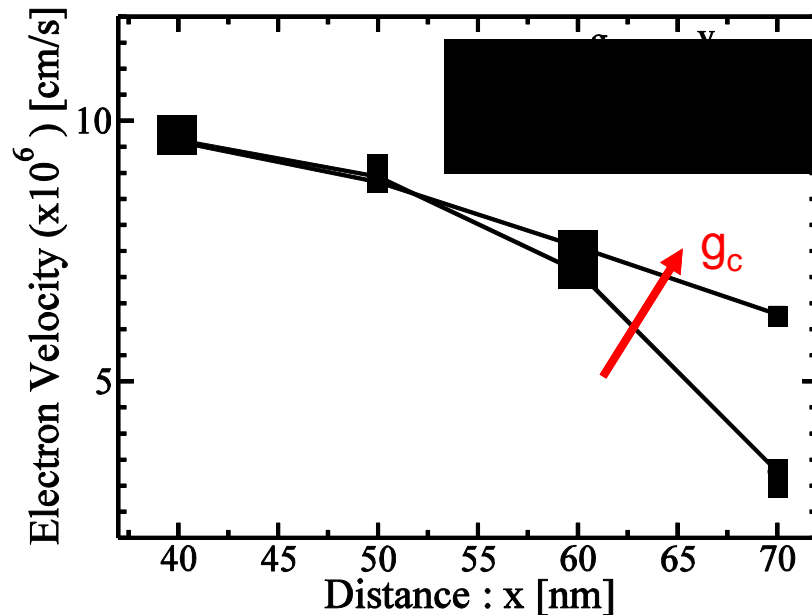
# Channel Transport in nTFET: Toy model



- The  $g_c$  and  $g_v$  in the tunneling model are artificially increased (by the same factor)
- $I_{ON}$  is not proportional to  $g_c$  and  $g_v$  for  $I_{ON}$  larger than few  $\mu\text{A}/\mu\text{m}$
- $I_{ON}$  increases with  $v_{sat}$  ( $\mu_e$  and  $\beta$  have negligible impact)

# Electrostatic Feedback: $N_{INV}$ and Velocity

Source-channel junction at 30nm and Drain-channel junction at 80nm

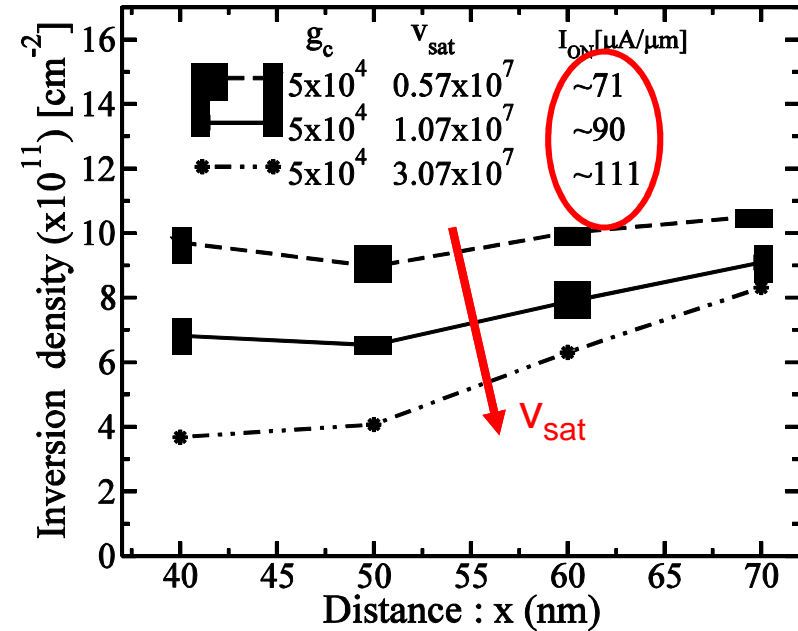
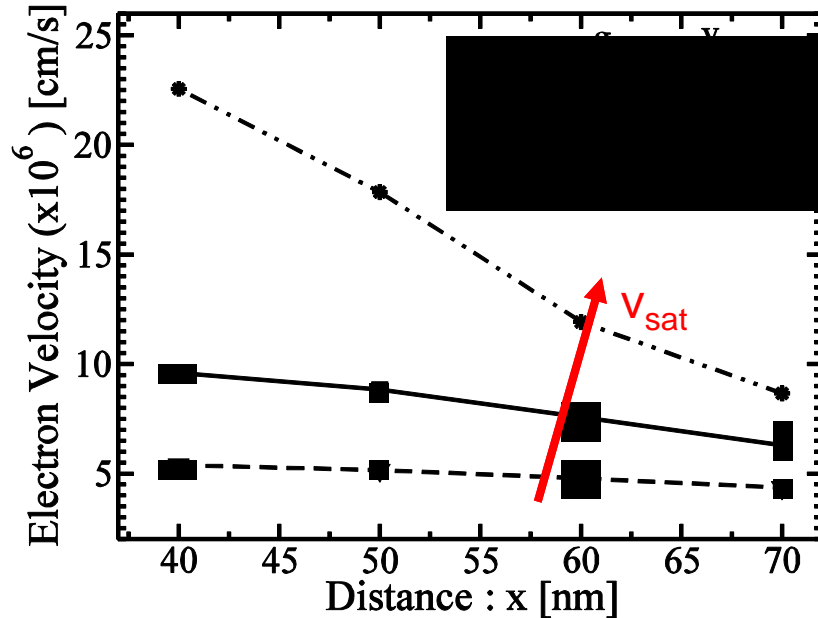


- Electric field at source side is high  $\rightarrow$  carriers velocity is saturated
- Electric field at drain side is low  $\rightarrow$  the carriers velocity reduces and  $N_{inv}$  increases towards the drain (marked difference w.r.t. MOSFETs)
- As the  $g_c$  value is increased the generation rate and  $N_{inv}$  increase

**Band edges are pushed upward  $\rightarrow$  electrostatic feedback**

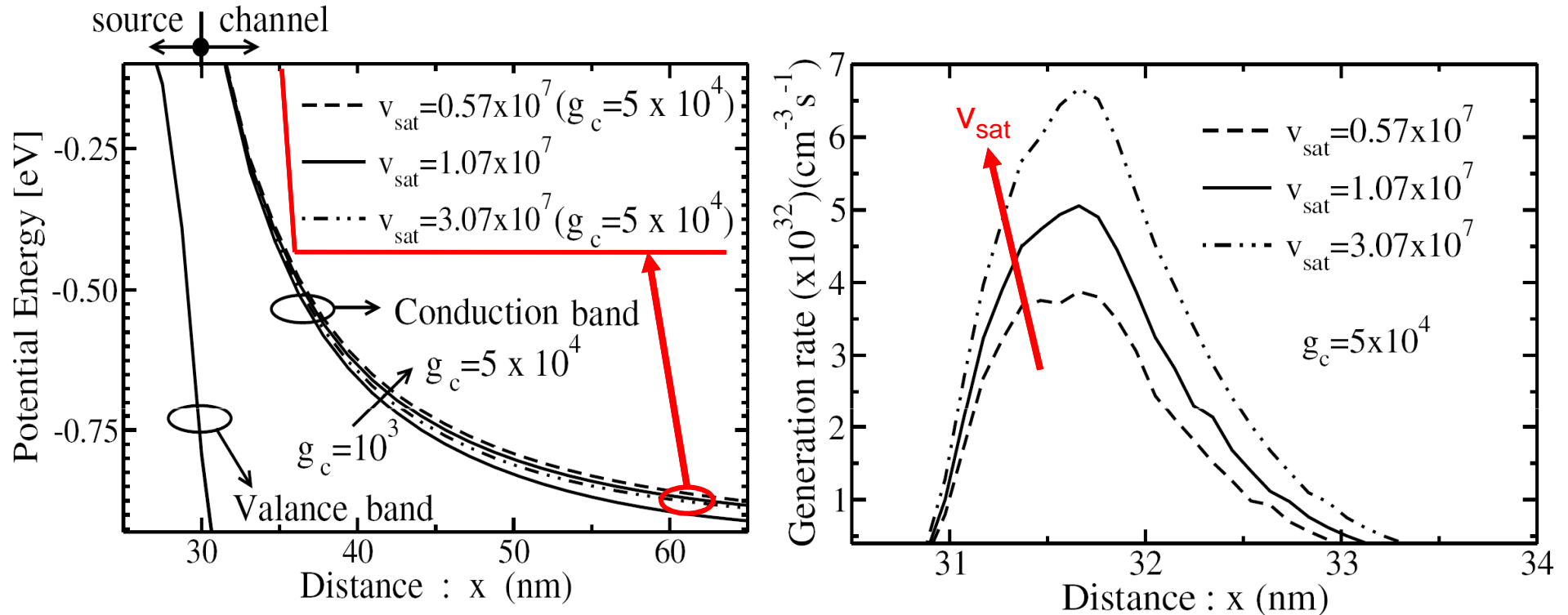
# Electrostatic Feedback: the role of carrier velocity

Source-channel junction at 30nm and Drain-channel junction at 80nm



- For a given generation rate ( $g_c$  value) the  $N_{inv}$  decreases for larger electron velocities
- Increasing carrier velocity is supposed to reduce the electrostatic feedback on the generation rate and thus to enhance  $I_{ON}$

# Electrostatic Feedback and carrier velocity



- Increase of generat. rate pushes the band edges upward
- As electron velocity increases the electrostatic feedback decreases, hence the generation rate and the  $I_{ON}$  improve

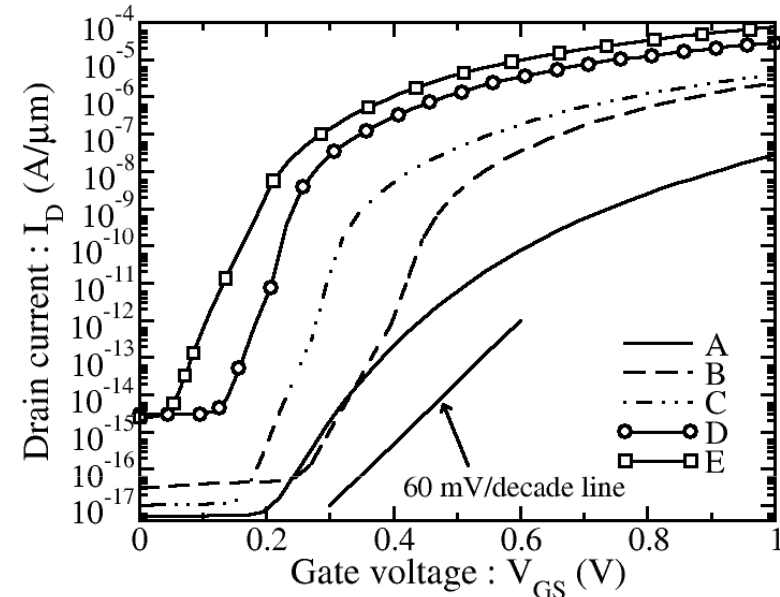
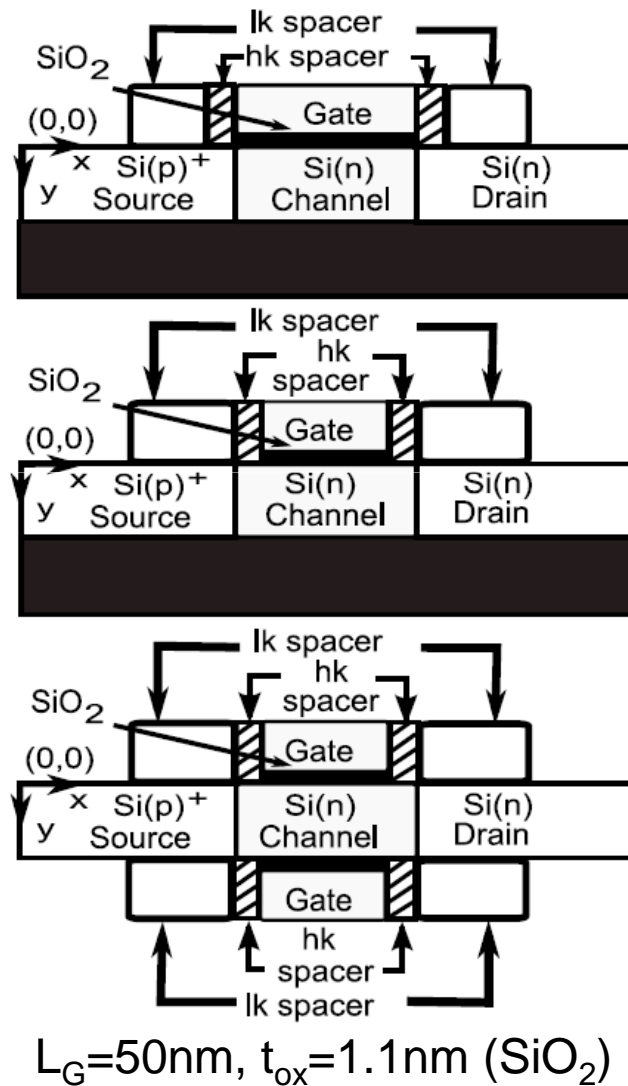


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# Channel Transport in nTFET: Technology Boosters

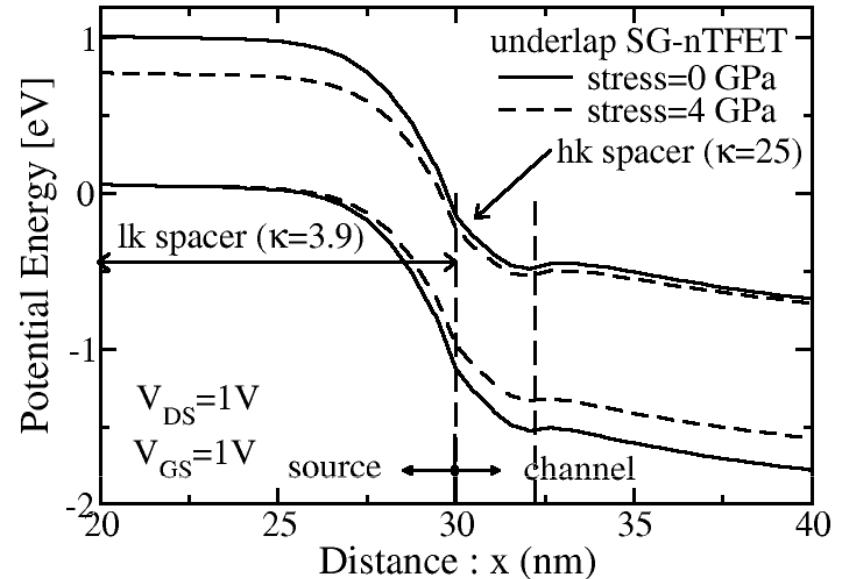


- A → nTFET with  $\text{SiO}_2$  spacer
  - B → nTFET with dual-k spacer
  - C → nTFET with underlap and dual-k spacer
  - D → same as C with 4GPa stress
  - E → same as D with double gate
- (see H. Virani *et al.* accepted for TED, 2010)

# Band Diagram : Technology Boosters

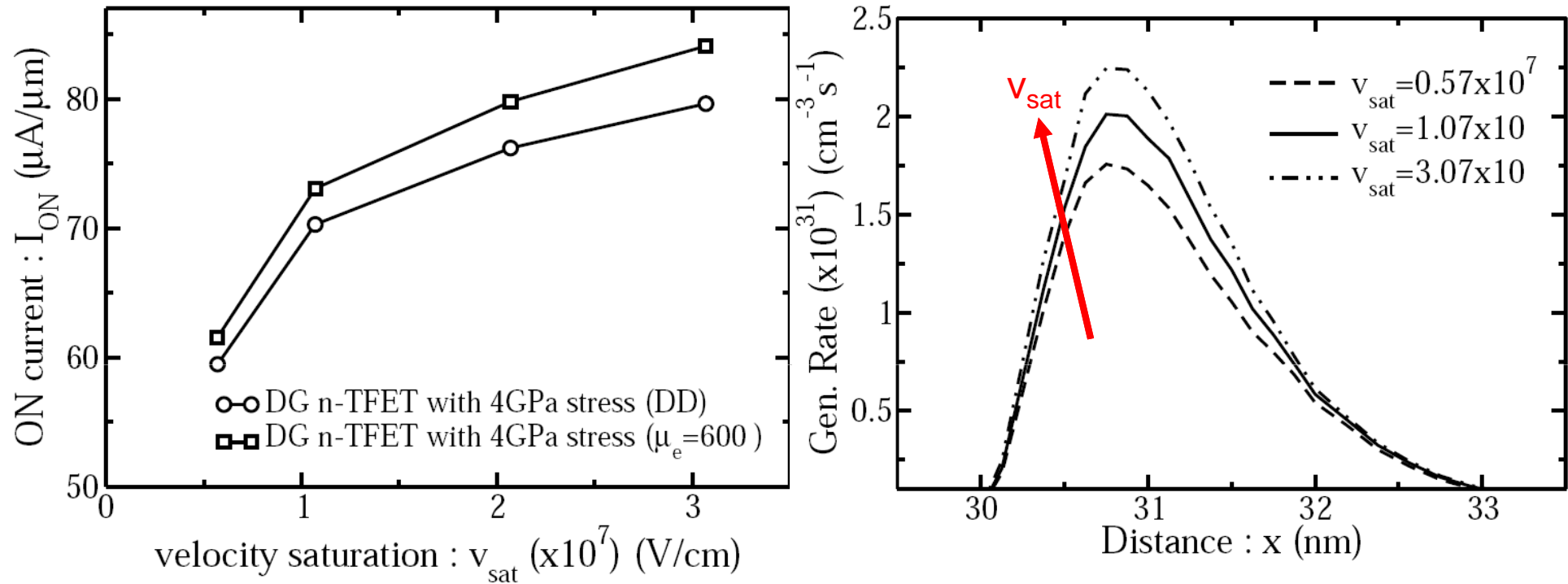
Stress (GPa)	Conduction Band (eV)	Valence Band (eV)	Bandgap (eV)
0	1.170	0	1.170
1	1.149	0.027	1.122
2	1.121	0.054	1.067
3	1.085	0.081	1.004
4	1.043	0.108	0.935

- Conduction band edge: after E.Ungersboeck et al. TED 2007
- Valence band: six-by-six k-p calculations



- Dual-k spacer produces additional band bending at source-channel junction (due to enhanced fringe field) and reduces the tunnelling distance (see H.G.Virani *et al.* TED, 2010)
- Further reduction of the tunnelling distance is obtained by a uniaxial stress in the  $\langle 110 \rangle$  source-drain direction of a (100) TFET

# Channel Transport in nTFET: Technology Boosters



- As velocity increases the electrostatic feedback reduces, hence generation rate and  $I_{ON}$  increase
- Mobility has negligible effect on  $I_{ON}$  (neglected strain induced mobility modulation)





# A few remarks

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- Throughout the study we used changes in the velocity saturation to *exemplify* the effects of the carrier velocity
- Verification of the results with more adequate transport models would be interesting
- The electrostatic feedback effect may depend on the channel length of the TFETs → *under investigation*



# Conclusions

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- For  $I_{ON} \geq \text{few } \mu\text{A}/\mu\text{m}$ , the tunneling generated electrons in nTFETs tend to accumulate in the channel and produce an electrostatic feedback which affects the  $I_{ON}$
- In this regime the  $I_{ON}$  becomes sensitive to the electron velocity and increases with it
- The tunneling barrier is the most important ingredient but not the only ingredient for the  $I_{ON}$  optimization
- III-V materials or graphene based devices may help *also in terms* of carrier velocity in the channel



# Acknowledgements

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- H.Virani, P.Palestri, L.Selmi, A. Kottantharayil
- This study partially funded by the italiani MIUR through the “Bando per borse a favore di giovani ricercatori indiani”.