FP7 STEEPER

@ SISPAD workshop on:

Simulation and Characterization of Steep-Slope Switches

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Outline

- Steeper: summary & status
- Partnership
- Goals & Objectives
- 1st year objectives and challenges

Goal and objectives (1)

General

OBJ 1: Demonstrate energy efficient steep subthreshold slope transistors based on quantum mechanical band-to-band tunneling (tunnel FETs) able to reduce the voltage operation of advanced nanoelectronic circuits into sub-0.5V and their power consumption by one order of magnitude.

OBJ 2: Enable and demonstrate the power consumption benefits resulting from hybridization of tunnel FET and CMOS technologies and from tunnel FETs as stand-alone technology for digital, analog, RF and mixed-mode circuit applications.

Technology

OBJ 3: Develop a CMOS-compatible UTB SOI technology platform for tunnel FETs with ultra-low standby power by exploiting key additive boosters for enhanced performance: high-k dielectrics, SiGe source, strain.

OBJ 4: Study and identify advanced technology implementations for high-Ion tunnel FETs: III-V materials, nanowires, staggered versus broken band gaps, electrostatic doping.

Goal and objectives (2)

Simulation and modelling

- **OBJ 5**: Develop accurate numerical simulation tools: semi-classical multi-sub-band Monte Carlo simulator and full-band quantum-transport simulation for in-depth study of UTB and nanowire tunnel FETs, respectively.
- **OBJ 6**: Study the scaling, parameter sensitivity and variability on the characteristics of nanometer tunnel FETs.
- **OBJ 7**: Develop and implement DC and AC compact models for the simulation and design of circuits based on tunnel FETs and or co-design with advanced CMOS.

Industrial benchmarking: device and circuit

- **OBJ 8**: Benchmark tunnel FETs developed in STEEPER for low standby power logic, high speed, memory, RF and analog applications. Evaluate their energy efficiency against CMOS.

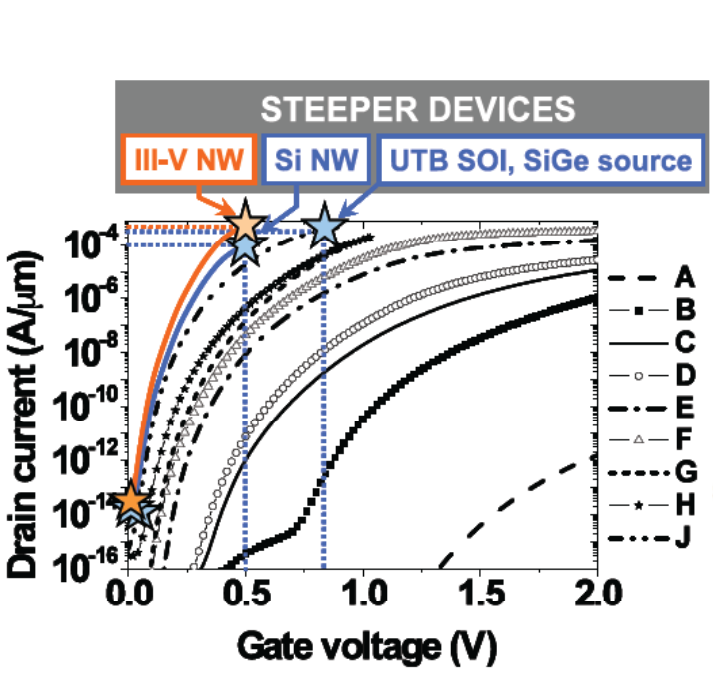
Partnership

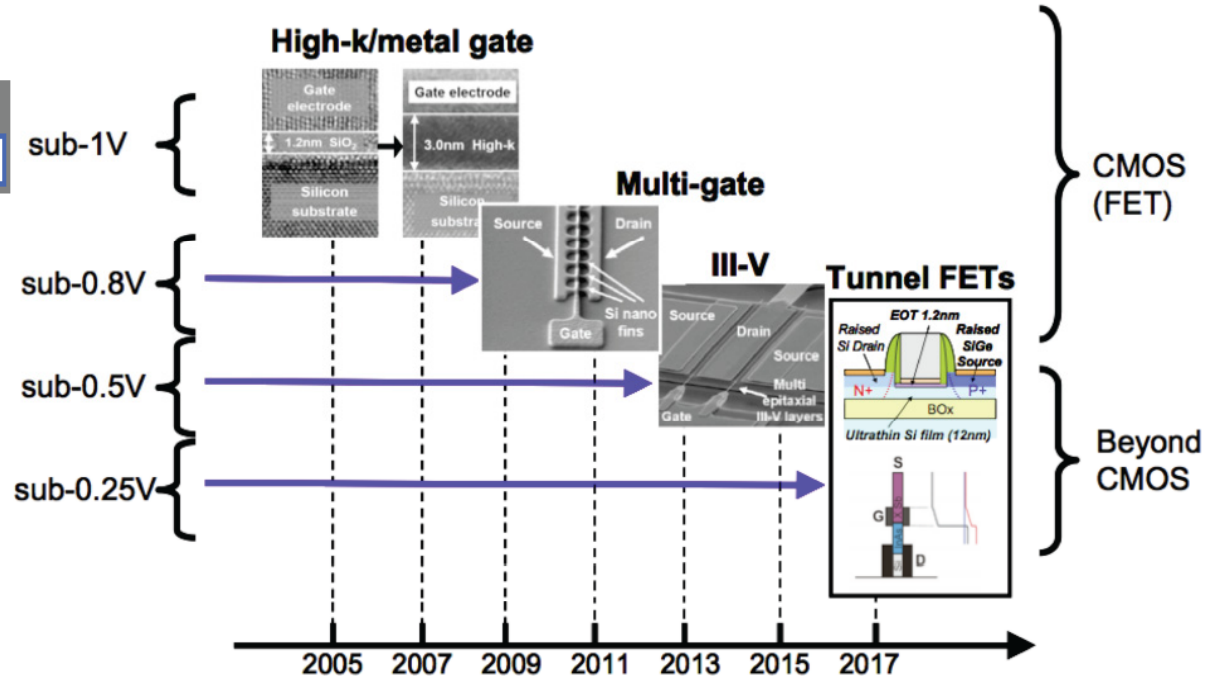
- 3 industries, 2 research institututes, 5 universities, 1 SME
- 4 countries: Germany, France, Italy, Switzerland.

Beneficiary no.	Beneficiary legal name	Country	Type of Beneficiary
1 (Coord.)	Ecole Polytechnique Fédérale de Lausanne (EPFL)	CH	University
2	Commissariat à l'Energie Atomique - Laboratoire d'Electronique et de Technologie de l'Information (CEA-LETI)	FR	Research centre
3	Consorzio Nazionale Interuniversitario per la Nanoelettronica (IUNET)	IT	University
4	Global Foundries (GF)	DE	Industrial
5	IBM Research GmbH, Zurich Research Laboratory (IBM-ZRL)	CH	Industrial
6	Infineon Technologies (INFINEON)	DE	Industrial
7	Research Center Juelich (FZJ)	DE	Research centre
8	SCIPROM Sàrl (SCIPROM)	CH	SME
9	Techniche Universität Dortmund (TU-D)	DE	University

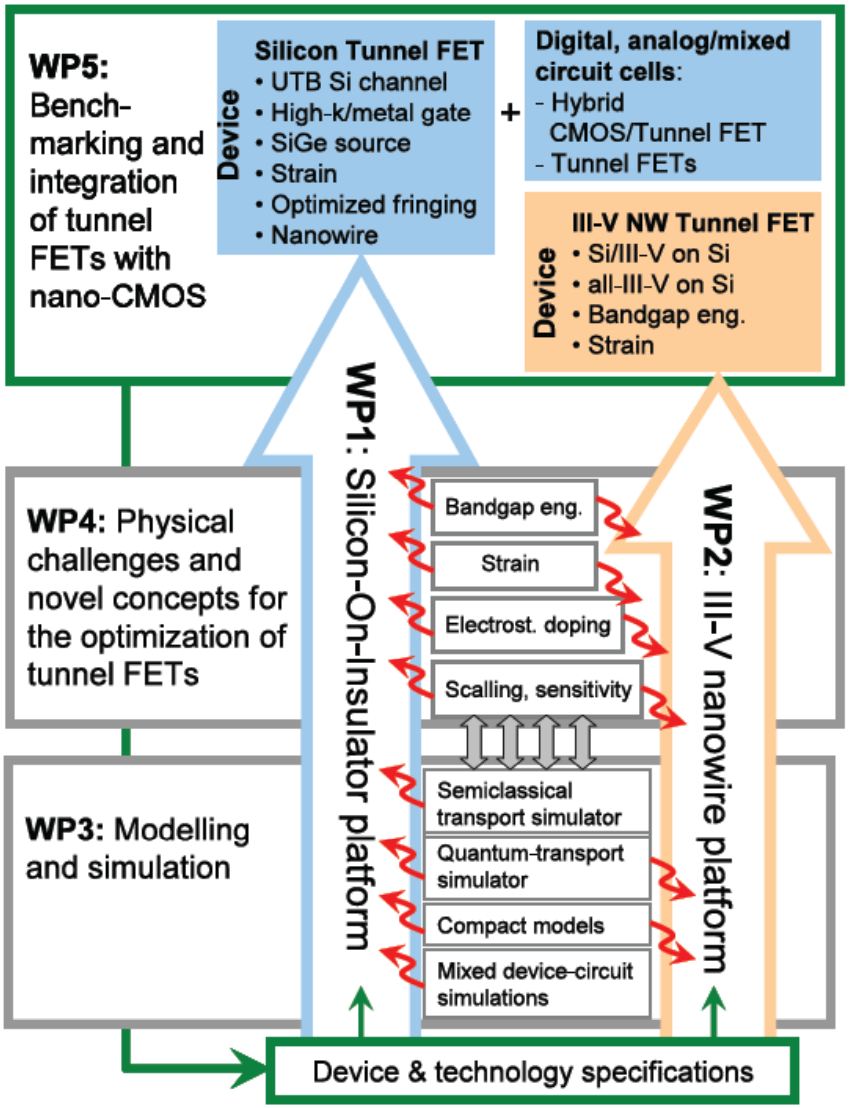
Progress beyond SOA

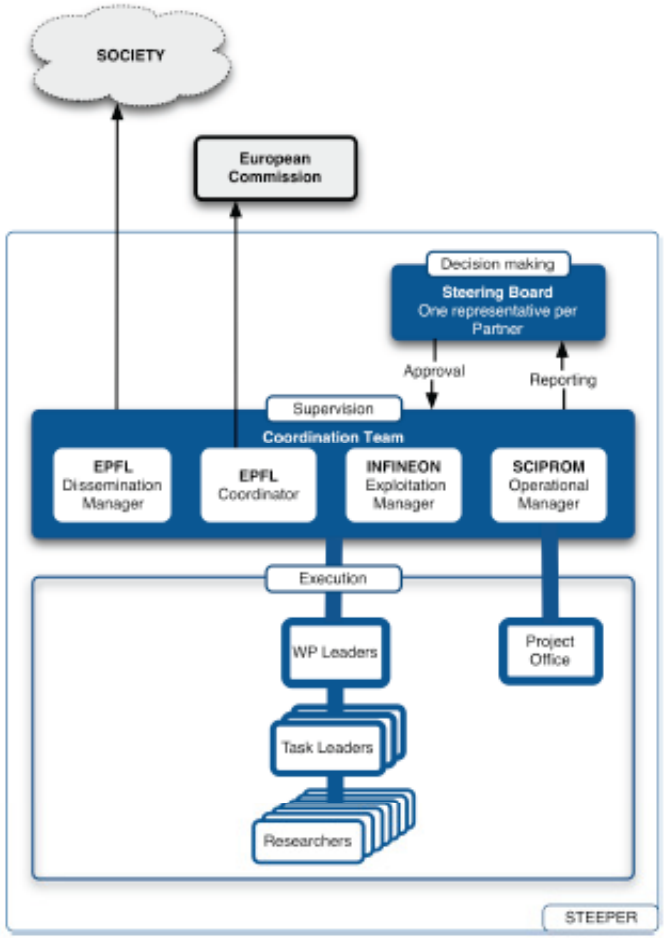
Objectives of the call	Objectives of the proposal
Objective ICT-2009.3.1: Nanoelectronics Technology: This objective focuses on the 'beyond CMOS' field, the advanced aspect of the 'More than Moore domain', their integration and their interfacing with existing technology.	**1)** Tunnel FETs as energy efficient beyond CMOS based on a technology booster strategy as beyond CMOS devices addressing fundamental nano-CMOS power issues. **2)** Development of hybrid silicon platform co-integrating tunnel FETs and CMOS with sub-50nm feature size (sub-45nm nodes). **3)** Enabling co-design of CMOS and tunnel FET circuits.





Structure and governance





Thank you!