JARA Jülich Aachen Research Alliance

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JÜLICH FORSCHUNGSZENTRUM

Planar and Nanowire Si-TFETs

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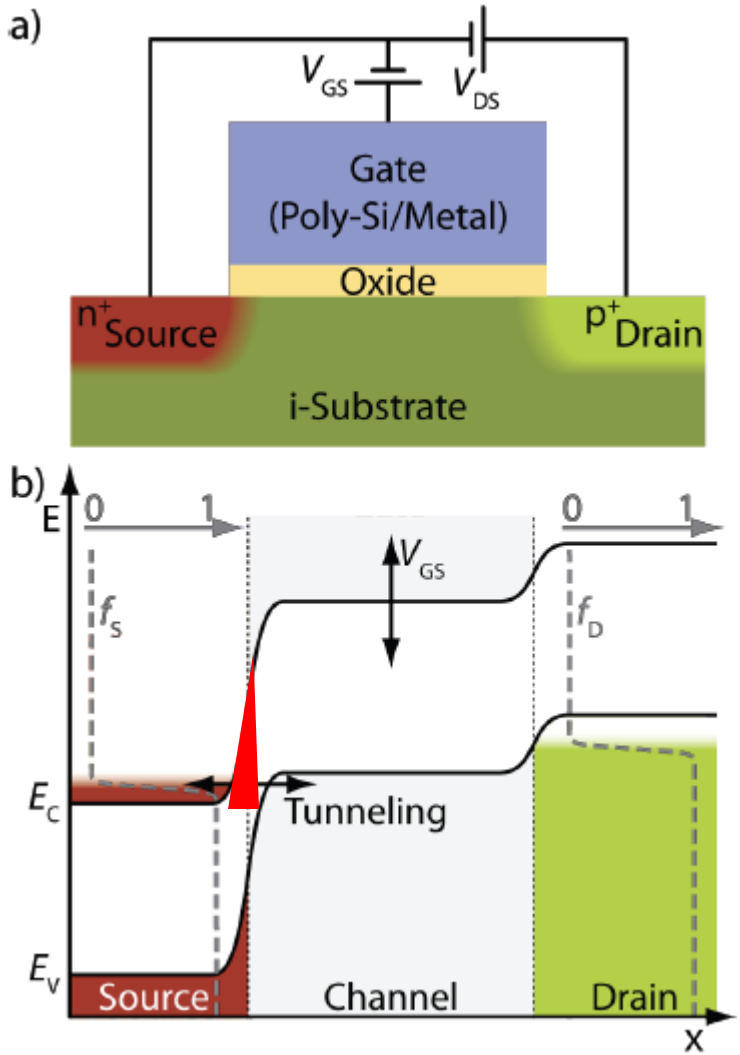
Outline

- Introduction
- Planar TFETs on SOI
- Planar TFETs on SiGe
- Nanowire Array TFETs
- Conclusions

TFET Structure + Modeling



- Drain current

$$I_D = \frac{2q}{h} W \int_{E_v^{ch}}^{E_c^S} T(E)[f_S(E) - f_D(E)]\, dE$$

- Transmission (WKB)
  - barrier approximated by triangular shape

$$T_{WKB} \approx exp\left(-\frac{4\Lambda\sqrt{2m^*}E_g^{3/2}}{3q\hbar(\Delta\Phi + E_g)}\right),$$

$$\Delta\Phi = E_v^{ch} - E_c^S$$

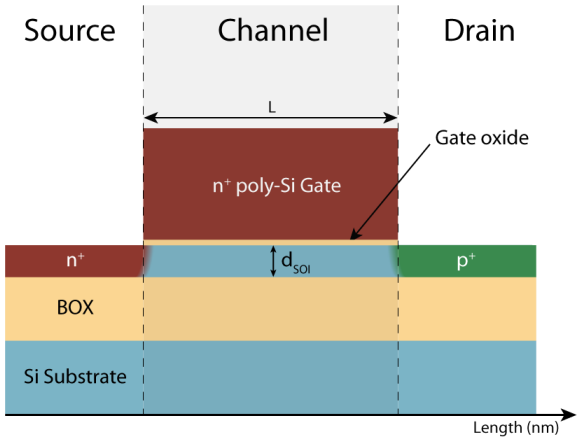
$$T \ll 1 \Rightarrow S \approx \frac{\ln(10)}{q}\frac{3q\hbar(\Delta\Phi + E_g)^2}{4\Lambda\sqrt{2m^*}E_g^{3/2}}$$

$$T \approx 1 \Rightarrow S \approx \frac{\ln(10)}{q}\Delta\Phi$$

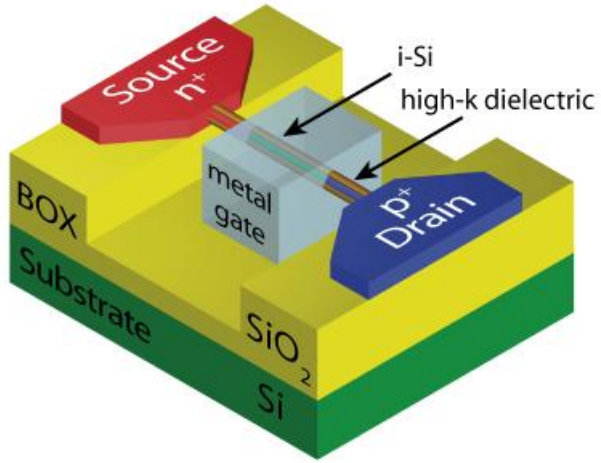
Optimization of T

- $T_{\mathrm{WKB}} \approx exp\left(-\frac{4\Lambda\sqrt{2m^*}E_g^{3/2}}{3q\hbar(\Delta\Phi + E_g)}\right)$
- $m^*, E_g \Rightarrow$ strained silicon, SiGe, germanium
- $\Lambda \Rightarrow$ Gate geometry and materials (e.g. high-κ)

$$\Lambda_{\mathrm{SOI}} = \sqrt{\frac{\epsilon_{\mathrm{Si}}}{\epsilon_{\mathrm{ox}}} d_{\mathrm{Si}} d_{\mathrm{ox}}}$$

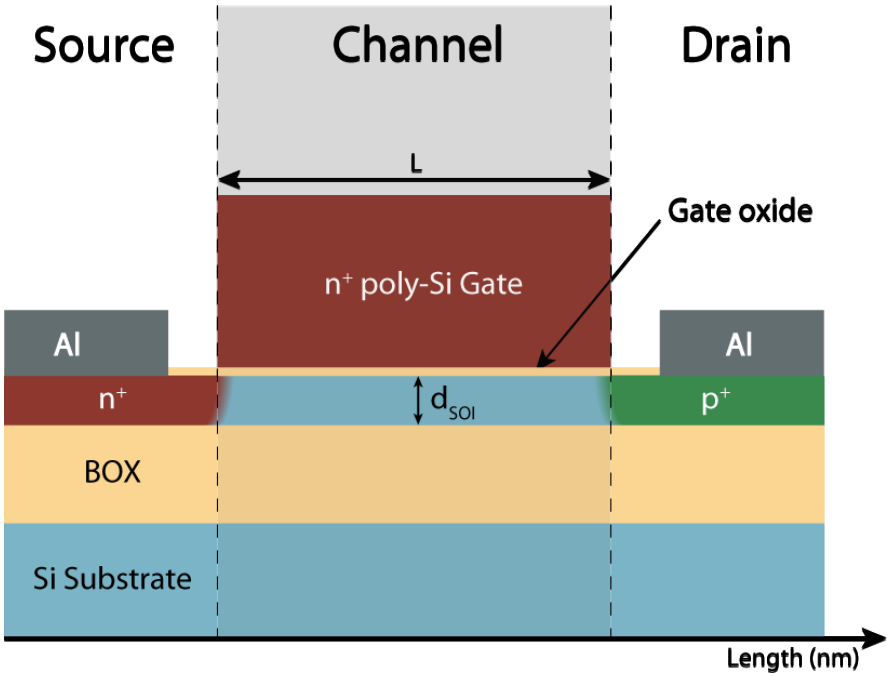


$$\Lambda_{\mathrm{NW}} = \sqrt{\frac{\epsilon_{\mathrm{NW}}}{8\,\epsilon_{ox}} d_{\mathrm{NW}}^2 \ln\left(1 + \frac{2d_{\mathrm{ox}}}{d_{\mathrm{NW}}}\right)}$$



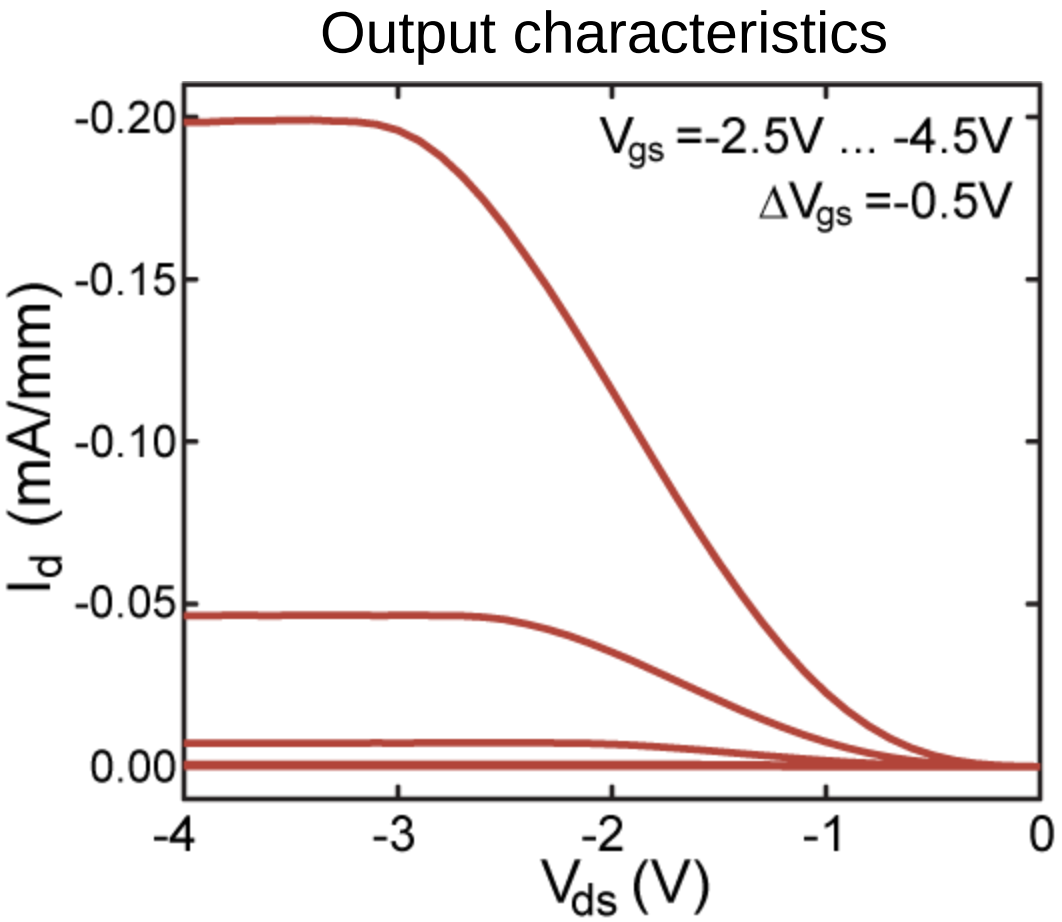
Planar TFET on SOI

- SOI substrate
  - d_{SOI} = 20 nm
  - d_{Ox} = 3.5 - 4.5 nm
- Gate lithography
  - Gate lengths: 2 - 12 µm
- Implantation
  - Dose: $3 \cdot 10^{15}$ /cm^2
  - Energy: 3-5 keV
- Activation
  - Spike anneal @ 1000°C



Output characteristics

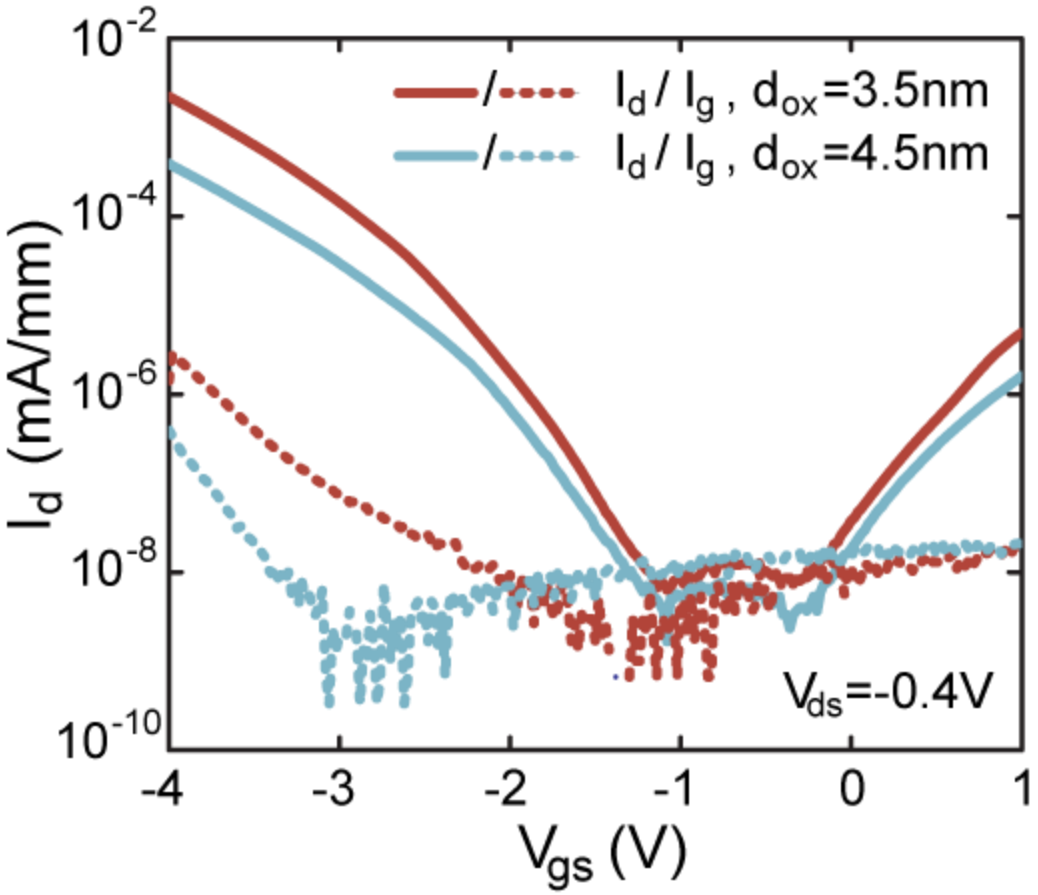
- Distinct saturation
- Exponential onset
- Current is limited by tunneling probability
- $\Lambda \approx 15$ nm



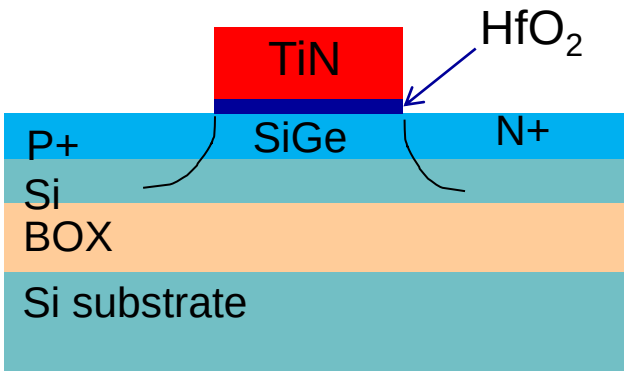
Gate oxide thickness scaling

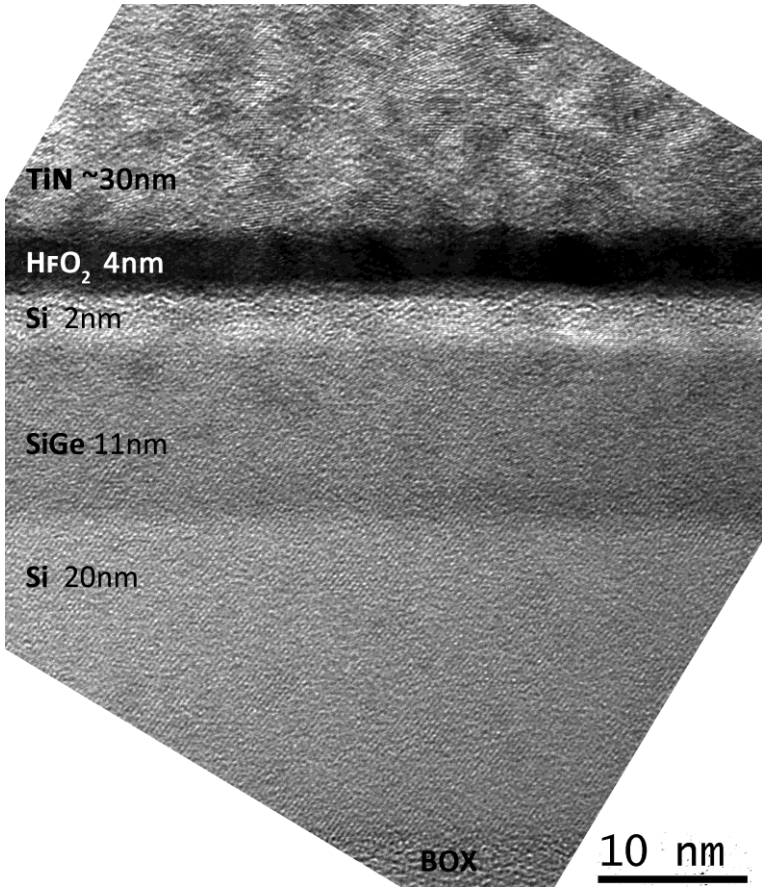
- 1 nm reduction of d_{ox} → $10 \cdot I_{D\ max}$
- S=300mV/dec

Transfer characteristics



Planar SiGe TFET





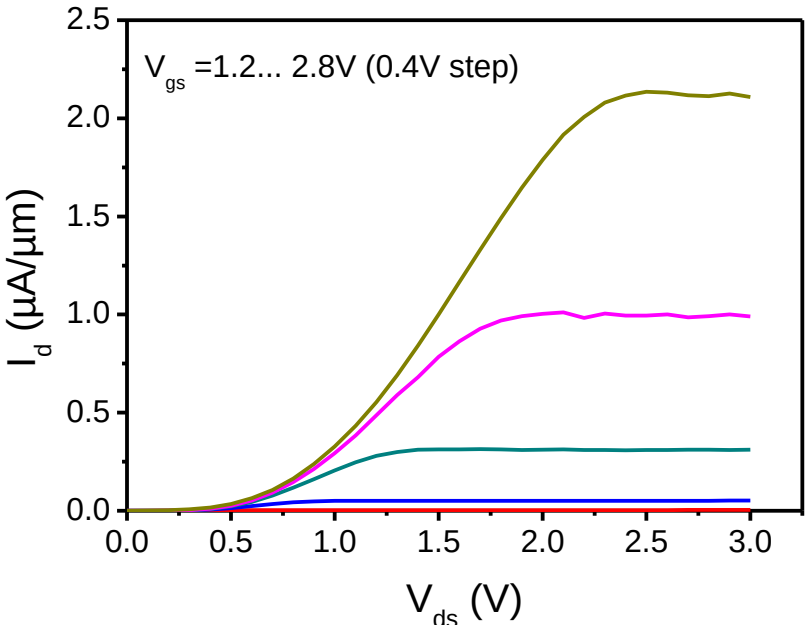
Compressively strained SiGe on SOI

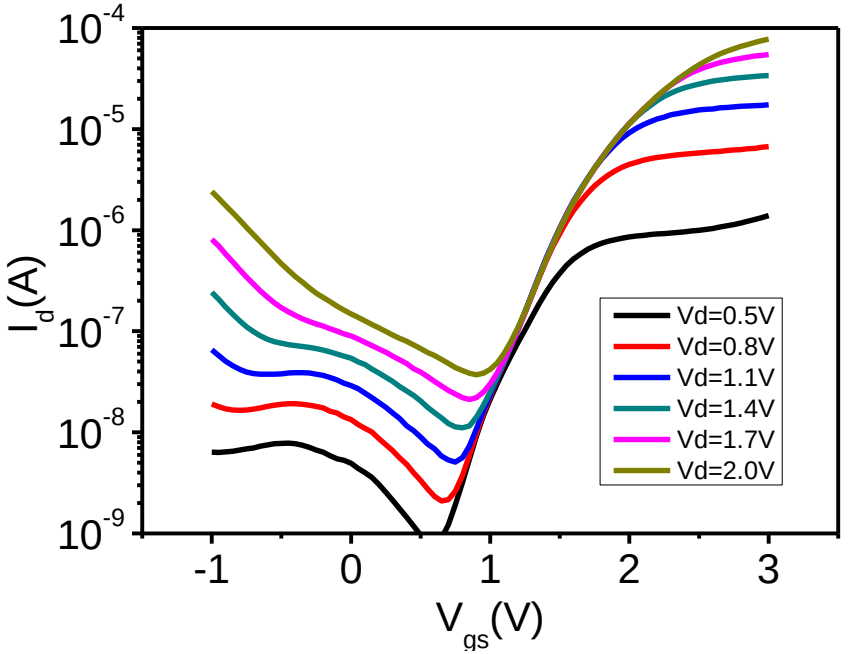
Ge content: X=0.35, 0.50, 0.65

SiGe Growth: J.-M. Hartmann, LETI

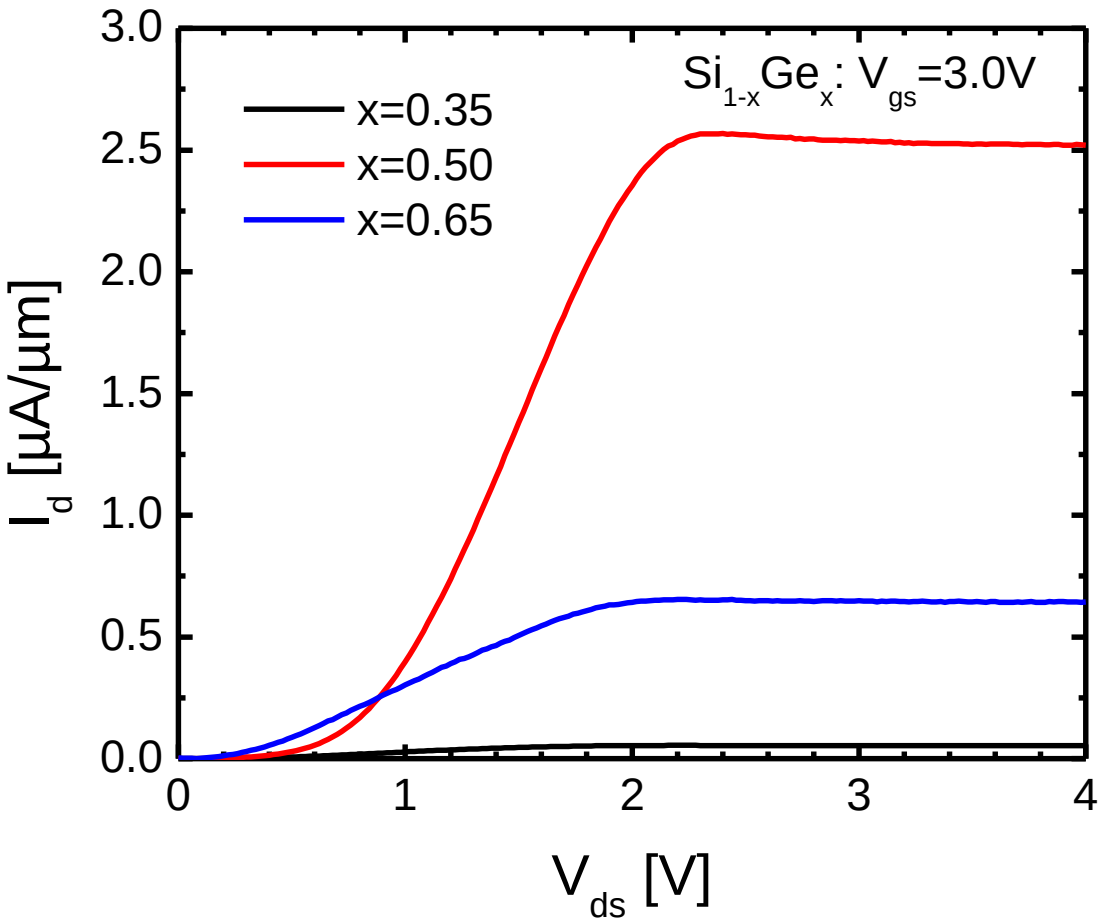
Planar SiGe n-TFET: 50%Ge

L/W=5/40

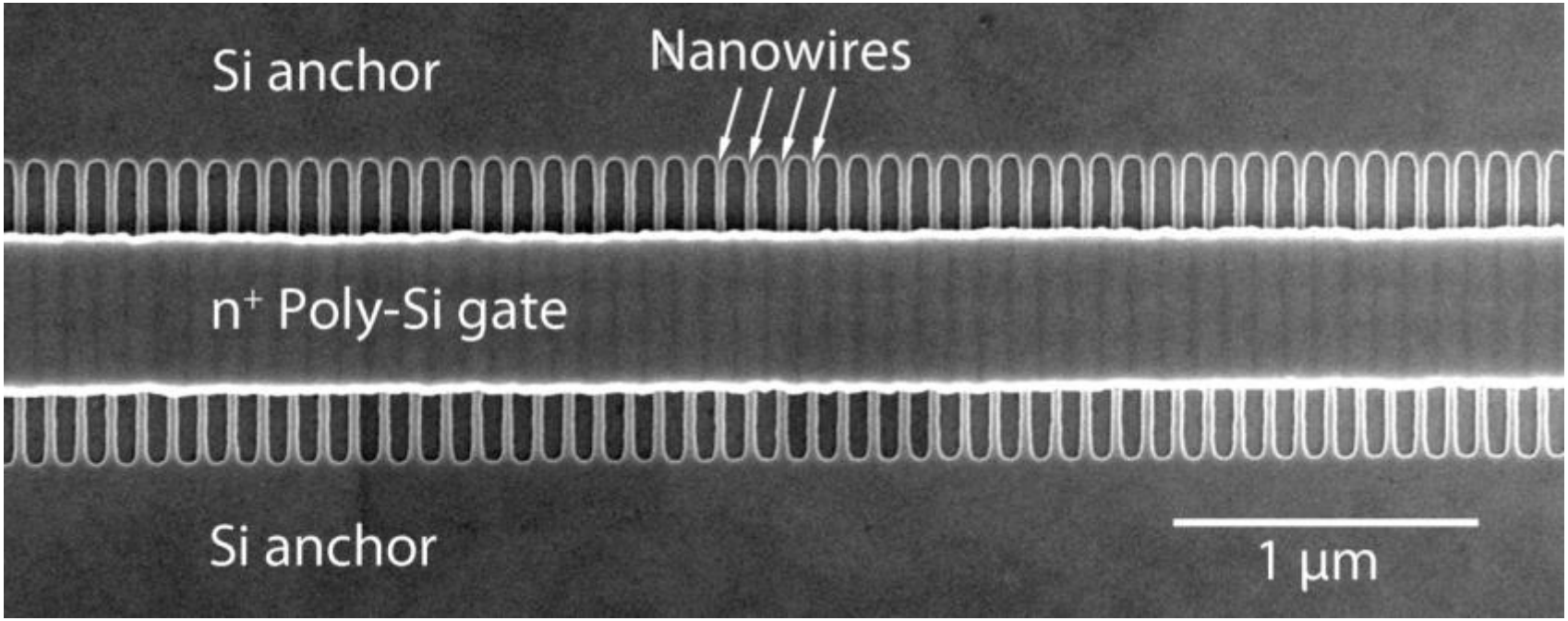




Planar SiGe TFET: Ge content effects

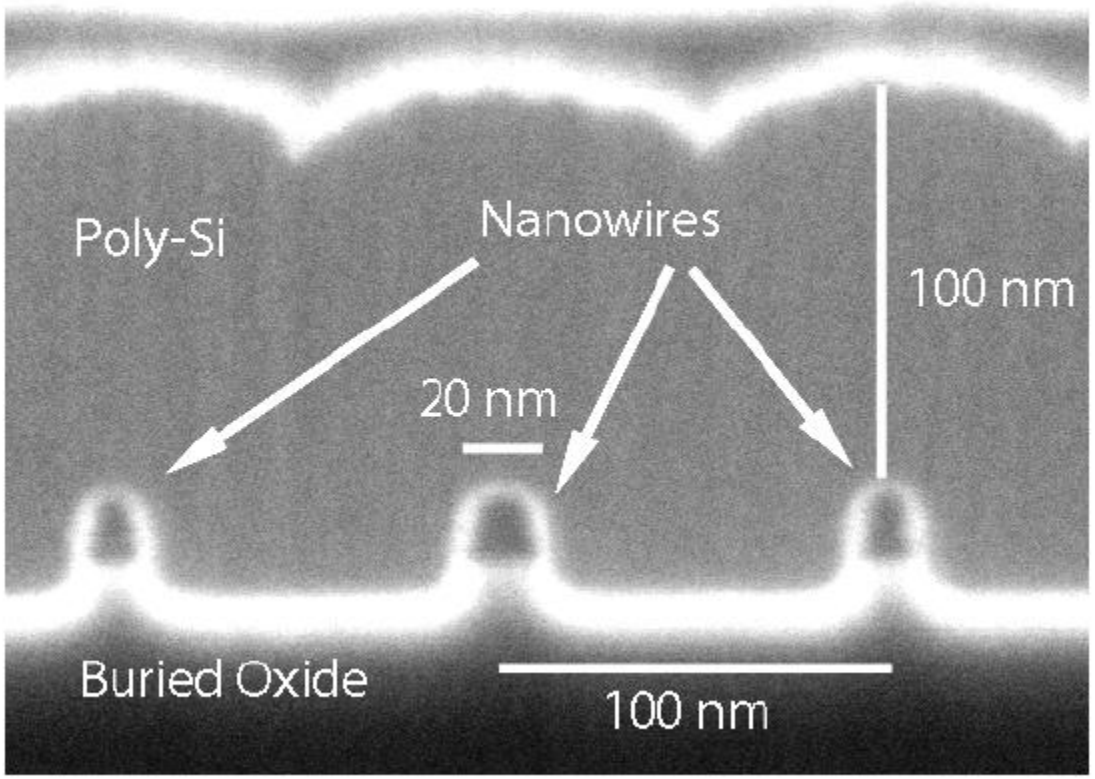


Nanowire array TFET - structure

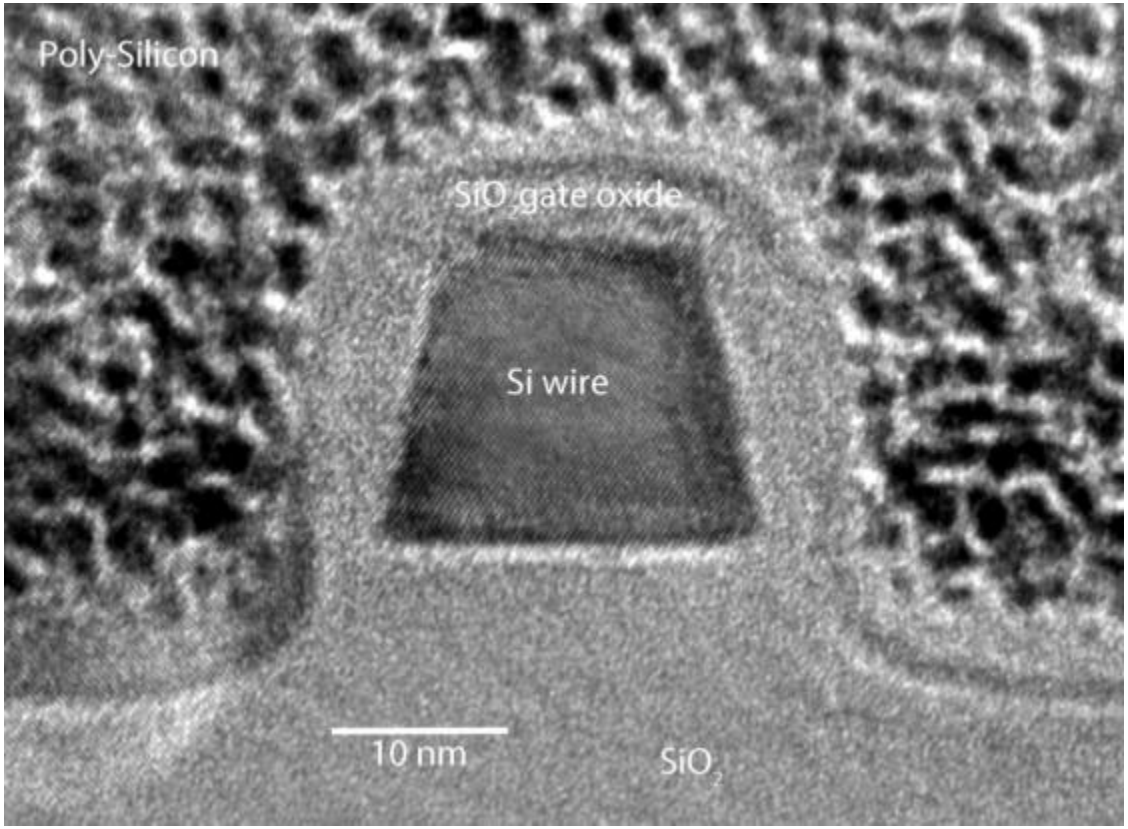


As^+ implantation: 5keV
B^+ implantation: 1.5keV
Spike annealing @1000°C

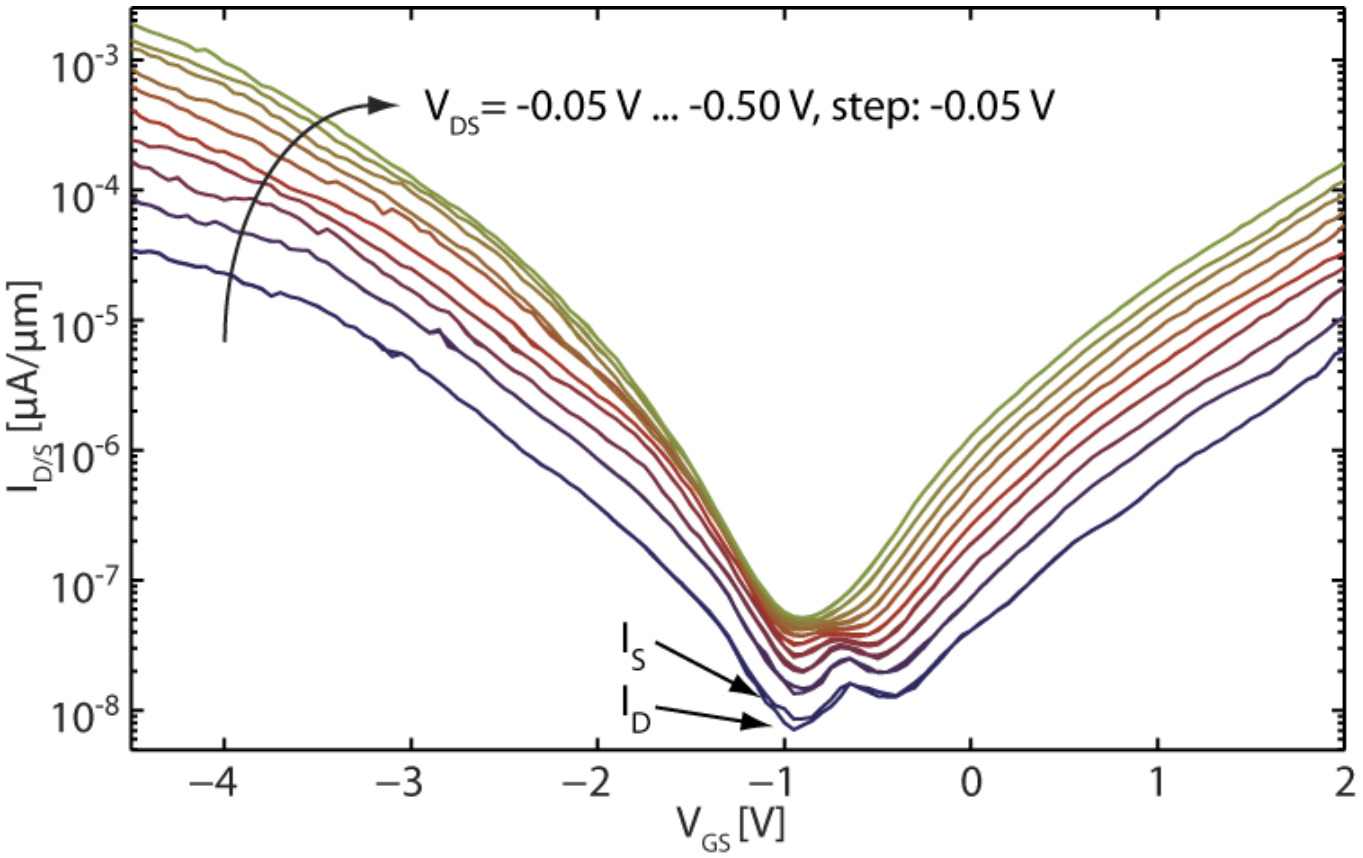
Nanowire array TFET - structure



Nanowire array TFET - structure

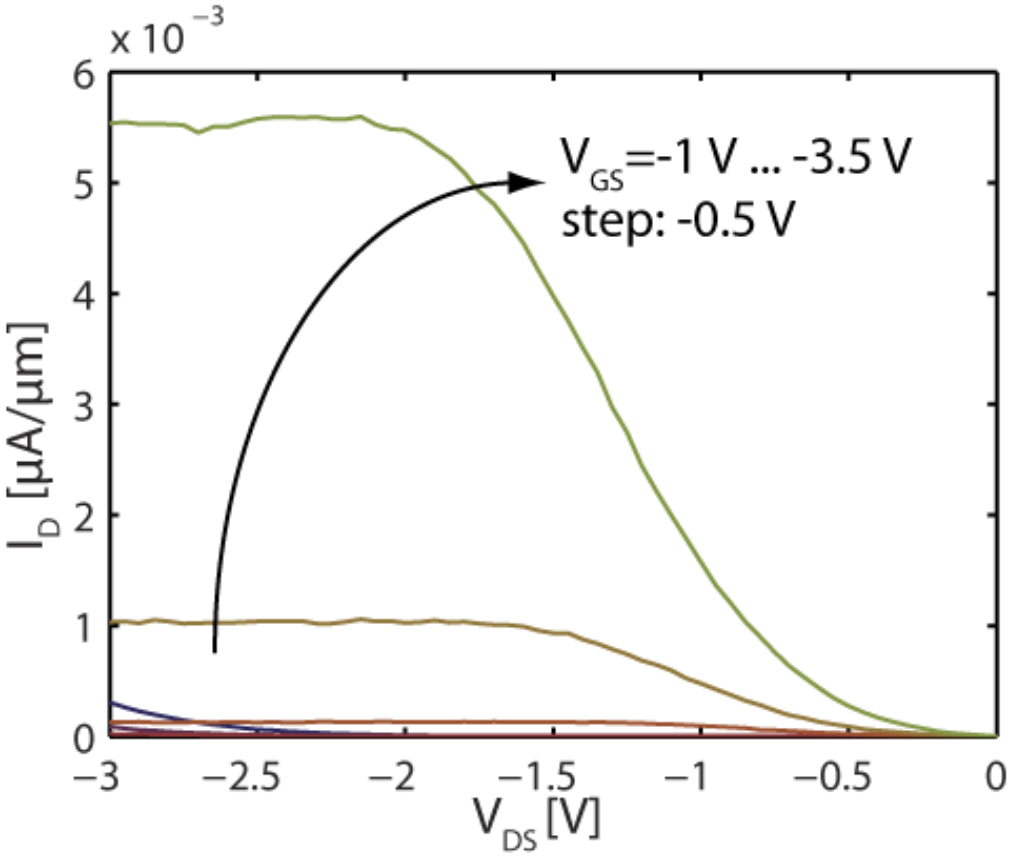


Transfer characteristics



Output characteristics

- Distinct saturation
- Exponential onset
- Currents nearly identical to SOI TFET!
- Λ ≈ 7 nm
  ➔ Why no improved currents?



- ➔ Electrostatics is better, but doping profile is not!

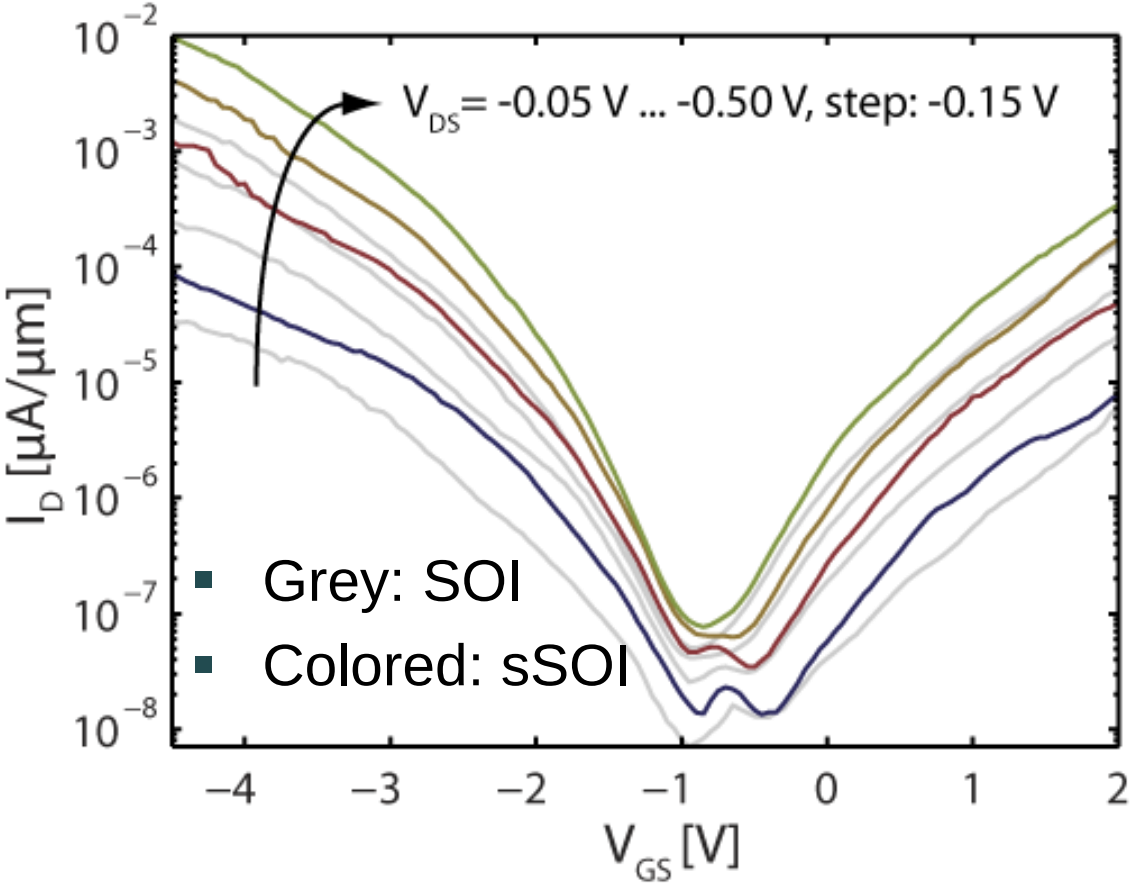
Strained Silicon – TFET

Biaxially tensile strained sSOI:

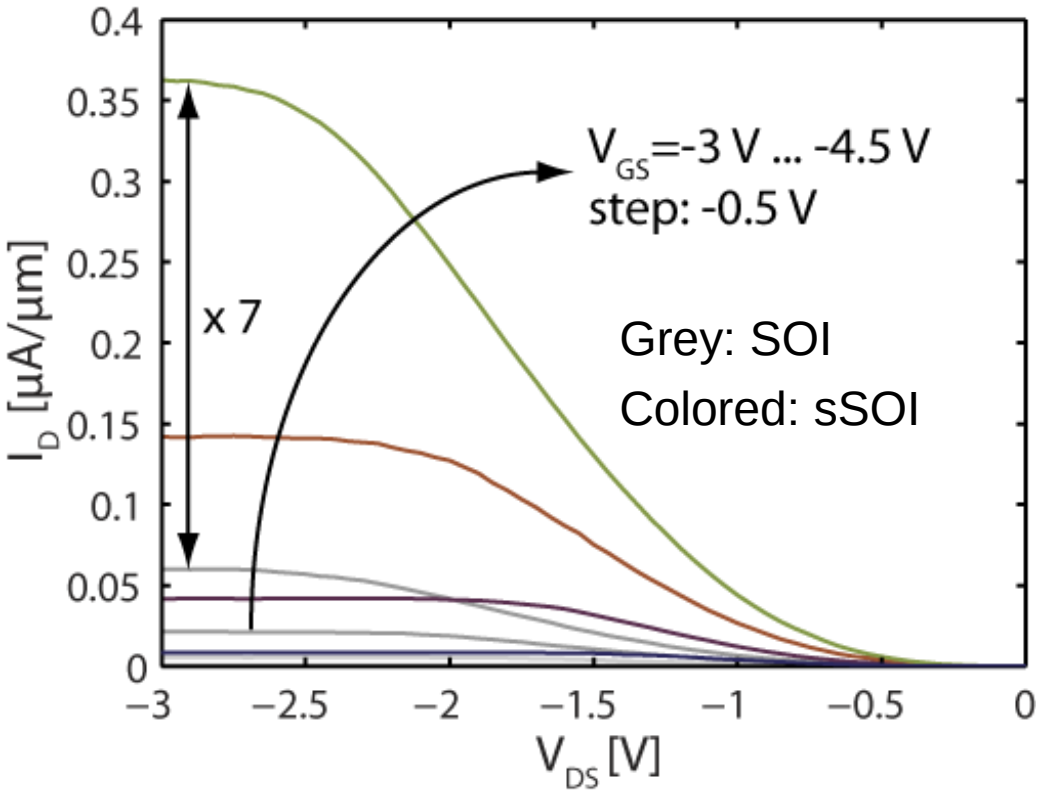
σ_{biax}=1.2 GPa

S= 375 mV/dec for SOI

S= 325 mV/dec for sSOI



Strained Silicon TFET - Output



$$T_{\mathrm{WKB}} \approx exp\left(-\frac{4\Lambda\sqrt{2m^*}E_g^{3/2}}{3q\hbar(\Delta\Phi + E_g)}\right)$$

sSOI:

- lower effective mass m^*.
- Smaller E_g: $\Delta E_g \approx 140\mathrm{meV}$

Lim et al., EDL , 2004

Implantation and annealing have to be optimized.

Conclusions

- Planar TFETs on SOI and Si/SiGe were fabricated.
- NW TFETs were achieved on SOI and SSOI
  SSOI enhances the current (7x).
- High-k materials and heterostructures improve the performance of TFETs considerably